IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellants:	Chul Woo Park, et al..	Confirmation No.	2186
Serial No.:	10/766,101	Art Unit:	2841
Filed:	January 28, 2004	Examiner:	Dinh, Tuan T.
For:	Double Mold Memory Card and Its Manufacturing Method		

SUPPLEMENTAL APPEAL BRIEF UNDER 37 C.F.R. § 41.37

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

Appellant [hereinafter "Appellant"], in the above-captioned patent application, has appealed from the Examiner's final rejection of Claims 1-24 as set forth in the Final Office Action of September 11, 2007.

A Notice of Appeal in response to the Final Office Action was filed on December 4, 2007. The Appeal Brief is being submitted electronically with the requisite fee under 37 C.F.R. § 1.17(c) in the amount of $510.00 having already been paid. An ORAL HEARING IS NOT REQUESTED.

If for any reason the necessary fee is not associated with this file, the Commissioner is authorized to charge the appropriate fee for the Appeal Brief and/or any necessary extension of time fees to Deposit Account Number 19-4330.

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I. REAL PARTY IN INTEREST

The real party in interest is Amkor Technology, Inc. by assignments recorded in the U.S. Patent and Trademark Office at Reel 014941, Frame 0706.

II. RELATED APPEALS AND INTERFERENCES

No related appeals and/or interferences are pending.

III. STATUS OF CLAIMS

Claims 1-24 currently pending in the present application have been finally rejected (see Appendix entitled "CLAIMS APPENDIX"), and are each currently on appeal.

IV. STATUS OF AMENDMENTS

There are no un-entered amendments.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The independent claims of the present application which are at issue in relation to the present Appeal are independent Claims 1, 11, 20, 21 and 22.

Independent Claim 1

Independent 1 is directed to a memory card 100 (Figures 1A, 1B; Paragraph 16) comprising a substrate 110 defining opposed, generally planar top and bottom surfaces 111, 112 and a plurality of terminals 113 disposed on the bottom surface 112 (Figure 1C;

Paragraph 16). An electronic component 120 is mounted to the top surface 111 of the substrate 110 (Figure 1C; Paragraph 17). Formed on the bottom surface 112 of the substrate 110 is a first encapsulation part 130 (Figure 1C; Paragraph 19). Formed on the top surface 111 of the substrate 110 is a second encapsulation part 140 which encapsulates the component 120 mounted to the top surface 111 of the substrate 110 (Figure 1C; Paragraph 20). The second encapsulation part 140 is completely separated from the first encapsulation part 130 by the substrate 110, with the first and second encapsulation parts 130, 140 each being exposed in the memory card 100 (Figure 1C).

Independent Claim 11

Independent Claim 11 is a method counterpart to independent Claim 1, and recites the initial step of providing a substrate 110 having opposed top and bottom surfaces 111, 112 and a plurality of terminals 113 disposed on the bottom surface 112 thereof (Figure 2A; Paragraph 22). In the next step of the method described in Claim 11, the first encapsulation part 130 is formed on the bottom surface 112 of the substrate 110 (Figure 2B; Paragraph 22). Thereafter, at least one electronic component 120 is mounted to the top surface 111 of the substrate 110 in a manner wherein the component 120 is electrically connected to the terminals 113 of the substrate 110 (Figure 2C; Paragraph 23). Finally, the second encapsulation part 140 is formed on the top surface 111 of the substrate 110 in a manner encapsulating the component 120 mounted thereto, the first and second encapsulation parts 130, 140 each being exposed in the memory card 100 and completely separated from each other by the substrate 110 (Figures 2D and 2E; Paragraph 23).

Independent Claim 20

Independent Claim 20 is similar to independent Claim 11 described above, and is also directed to a method of forming the memory card 100. Claim 20 differs from Claim 11 primarily in the substitution of the first and second encapsulation parts terminology in Claim 11 with the "mold compound" terminology in Claim 20 (Figures 2A-2E; Paragraph 19).

Independent Claim 21

Independent Claim 21 is similar to independent Claim 1 described above, and is also directed to the memory card 100. Claim 21 differs from Claim 1 by further describing the first encapsulation part 130 and the second encapsulation part 140 in terms of differing first and second thicknesses (Figures 1C, 2D and 2E; Paragraphs 19, 20).

Independent Claim 22

Independent Claim 22 is a method counterpart to independent Claim 21, and is also similar to independent Claim 20. In this regard, in Claim 22, the "mold compound" terminology is used, as is the description of the first encapsulation part 130 and the second encapsulation part 140 in terms of differing first and second thicknesses (Figures 1C, 2D and 2E; Paragraphs 19, 20).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(A) Whether independent Claims 1, 11, 20, 21 and 22 are improperly rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,988,668 to Osako et al. [hereinafter "OSAKO"].

In the Final Office Action mailed September 11, 2007 in relation to the subject patent application, the Examiner indicated that Claims 1, 2, 11, 12 and 20 were rejected under 35 U.S.C. §102(e) as purportedly being anticipated by OSAKO. However, based on the totality of the language included in Section 2 of the such Final Office Action, it appears that the Examiner actually intended to identify Claims 1, 2, 6-12 and 16-23 as being anticipated by OSAKO, with the opening paragraph of Section 2 thus being in error. This same issue arose in the prior Office Action of March 7, 2007, with Appellant's request for clarification as presented in the Amendment filed June 14, 2007 having been ignored by the Examiner in the Final Office Action of September 11, 2007. Appellant asked for clarification for a second time in its Response to Final Office Action filed November 8, 2007. This second request was also ignored by the Examiner in the Advisory Action rendered November 23, 2007. In any event, for purposes of this appeal, Appellant once again assumes that Claims 1, 2, 6-12 and 16-23 currently stand as rejected under Section 102(e) as being anticipated by OSAKO.

Additionally, in the Final Office Action mailed September 11, 2007 in relation to the subject patent application, the Examiner indicated that Claims 3 and 13 were rejected under 35 U.S.C. §103(a) as being unpatentable over OSAKO in view of HIRAI. However, based on the totality of the language included in Section 4 of such Final Office Action, it appears that the Examiner actually intended to identify Claims 3, 4, 13 and 14 as being unpatentable over OSAKO in view of HIRAI, with the opening paragraph of Section 4 also being in error. This same issue arose in the prior Office Action of March 7, 2007, with Appellant's request for clarification as presented in the Amendment filed June 14, 2007 having been ignored by the Examiner in the Final Office Action of September 11, 2007. Appellant asked for clarification for a second time in its Response to Final Office Action filed November 8, 2007.

This second request was also ignored by the Examiner in the Advisory Action rendered November 23, 2007. Once again, for purposes of this appeal, Appellant assumes that Claims 3, 4, 13 and 14 currently stand as rejected under Section 103(a) as being unpatentable over OSAKO in view of HIRAI.

VII. ARGUMENT

(A) Grouping of Claims

For the purpose of this appeal, Appellant submits that:

(1) Dependent Claims 2-10 and 23-24 stand or fall with underlying independent Claim 1; and

(2) Dependent Claims 12-19 stand or fall with underlying independent Claim 11.

(B) Traversal of Rejection under 35 U.S.C. § 102(e)

The rejection of independent Claims 1, 11, 20, 21 and 22 under 35 U.S.C. § 102(e) as being anticipated by OSAKO is in error, the rejection should be reversed, and the subject application should be remanded to the Examiner with instructions to allow all of the pending claims thereof.

A Review of OSAKO

As is apparent Figures 1-3 and 19-21 of OSAKO, the IC card 1 comprises a wiring substrate 5 have an interconnect 10 formed on one side thereof, and an external connection terminal 6 formed on the side thereof opposite that having the interconnect 10 formed thereon. Attached to the side of the substrate 5 having the interconnect 10 formed thereon is

a semiconductor chip 7. The semiconductor chip 7 is electrically connected to the interconnect 10 through the use of a bonding wire 9. The semiconductor chip 7, bonding wire 9, interconnect 10 and a portion of that surface of the substrate 5 to which the semiconductor chip 7 is mounted are covered by a sealing portion 8 made of a thermosetting resin material. A portion of the remaining side of the substrate 5 having the connection terminal 6 formed thereon is covered with a sealing portion 3 which is made of a thermoplastic resin material.

As is explained in the specification of OSAKO and shown in the above-referenced figures thereof, the majority of the sealing portion 8 is covered by a case 2 as a result of the fitting of the sealing portion 8 into a complimentary dent or recess 2a defined by the case 2. That portion of the sealing portion 8 which is not covered by the case 2 is itself covered by the subsequently formed sealing portion 3, the case 2 and the sealing portion 3 being described as made of the same thermoplastic resin material. In this regard, the explicit teaching of OSAKO is that the IC body 4 collectively defined by the substrate 5, semiconductor chip 7, bonding wire 9 and sealing portion 8 is cooperatively engaged to the case 2 by the sealing portion 3, with a portion of the surface of the substrate 5 having the connection terminal 6 formed thereon and at least a portion of the surface of the case 2 on the side on which the IC body 4 is mounted being covered with the sealing portion 3 (OSAKO, column 5, line 66 through column 6, line 10).

Independent Claims 1, 11 and 20-22 are Not Anticipated by OSAKO

Appellant respectfully submits that independent Claims 1, 11 and 20-22 are not anticipated by OSAKO. In their current form, independent Claims 1, 11 and 21 each

describe the first and second encapsulation parts as each being ***"exposed in the memory card."*** Additionally, independent Claims 20 and 22 in their current form each describe the mold compound applied to the substrate in accordance with the recited memory card fabrication method as being ***"exposed in the memory card."***

In addition, in their current form, independent Claims 1, 11 and 21 each describe the first and second encapsulation parts as being ***"completely separated"*** from each other by the ***"substrate."*** Similarly, independent Claims 20 and 22 each describe the mold compound applied to the bottom surface as being ***"completely separated"*** from the mold compound applied to the top surface by the ***"substrate."***

Appellant respectfully submits that the clear teaching of OSAKO, as highlighted above, is that the external card shape of the IC card 1 is collectively defined by the case 2 and the sealing portion 3 thereof. In this regard, the sealing portion 8 is ***completely covered*** by the case 2 alone or in combination with the sealing portion 3, and thus is not exposed in the IC card 1 formed in accordance with any embodiment described in OSAKO. Moreover, as is seen in Figures 2, 21, 24, 31, 34, 36, 40, 46 and 47 of OSAKO, the case 2 and the sealing portion 3, which are each exposed in the IC card 1, are always in direct contact with each other.

In the Final Office Action of September 11, 2007 the Examiner correlates the "first encapsulation part" called out in the pending claims to the sealing portion 3, and correlates the "second encapsulation part" called out in the pending claims to the sealing portion 8. In this regard, the Examiner argues that the sealing portion 8 is ***"completely separated"*** from the sealing portion 3, and that the sealing portions 3, 8 are each ***"exposed in the memory card"*** (Final Office Action, page 3, lines 1-2 and 11-12).

Through the presentation of this argument, the Examiner appears to have retreated to the same position taken in the prior Office Action of August 22, 2006 rendered in relation to the subject application, wherein the Examiner characterized the sealing portion 8 of OSAKO alone as satisfying the "second encapsulation part" feature recited in each of Claims 1 and 11, and as further satisfying the mold compound applied to the top surface of the substrate as recited in step (d) of Claim 20. Appellant addressed this argument in its prior Amendment of December 6, 2006, wherein Appellant first established that the sealing portion 8 of OSAKO is ***completely covered*** by the case 2 alone or in combination with the sealing portion 3, and thus is not exposed in the IC card 1.

In apparent acceptance of the Appellant's argument presented in the prior Amendment of December 6, 2006 that the sealing portion 8 of OSAKO is completely covered by the case 2 alone or combination with the sealing portion 3 and thus is not exposed in the IC card 1, in the prior Office Action of March 7, 2007, the Examiner changed directions and characterized ***the combination*** of the sealing portion 8 ***and*** the case 2 as purportedly satisfying the "second encapsulation part" feature recited in each of Claims 1, 11 and 21, as well as the mold compound applied to the top surface of the substrate as recited in step (d) of each of Claims 20 and 22.

In its Amendment of June 14, 2007, Appellant responded to this reformulated argument by demonstrating that the clear, explicit teaching of OSAKO is that only the sealing portion 8 ***"encapsulates"*** the semiconductor chip 7 in accordance with the accepted meaning of the term in the relevant art, and that the specification of OSAKO actually states that the ***"sealing portion 8"*** is used for ***"sealing the semiconductor chip 7"*** (OSAKO, column 5, lines 33-34). In this regard, Appellant established that there is absolutely no

teaching or suggestion in OSAKO regarding the case 2 as ***"encapsulating"*** the semiconductor chip 7 since only the sealing portion 8 does, and further established that though the sealing portion 8 encapsulates the semiconductor chip 7, it is clearly not exposed in the IC card 1, unlike the case 2 which is exposed therein. Appellant also demonstrated that the element formed by the combined sealing portion 8 and case 2 is not ***"completely separated"*** from the sealing portion 3 since the sealing portion 3 and case 2 are always in contact with each other.

Now, as indicated above, the Examiner has again changed direction in the Final Office Action of September 11, 2007 by advancing the same position taken in the prior Office Action of August 22, 2006, despite having previously retreated from that position in the prior Office Action of March 7, 2007. However, the Examiner's current argument again ignores the clear, explicit teachings of OSAKO, with the basic premise of such argument regarding the applicability of the teachings of OSAKO to the features of Claims 1, 11 and 20-22 continuing to be fundamentally flawed.

More particularly, as indicated above, in each of independent Claims 1, 11 and 20-22, the first and second encapsulation parts (in the case of Claims 1, 11 and 21) or the mold compound (in the case of Claims 20 and 22) are each described as being "***exposed***" in the memory card. Contrary to the Examiner's current argument, the sealing portion 8 of OSAKO, correlated by the Examiner to the ***"second encapsulation part"***, is simply not ***"exposed"*** in the IC card 1. Appellant notes that in the current rejections of Claims 20 and 22, the Examiner makes reference to the "first and second encapsulation parts" features, despite such language not appearing in either of these claims.

Thus, Appellant respectfully submits that independent Claims 1, 11 and 20-22 are not anticipated by OSAKO, and are in condition for allowance. Additionally, Appellant respectfully submits that Claims 2-10, 12-19, 23 and 24 are also in condition for allowance as being dependent upon respective allowable base claims.

VIII. CONCLUSION

In view of the foregoing, it is submitted independent Claims 1, 11 and 20-22 are not anticipated by OSAKO, and are in condition for allowance. Additionally, Appellant respectfully submits that each and every pending claim of the present invention meets the requirements for patentability under 35 U.S.C. §§102 and 103, and requests that all of the aforementioned rejections be reversed by the Board, and that the application be remanded to the Examiner for withdrawal of all the rejections.

Accordingly, allowance of the present application and all the claims therein is respectfully requested and believed to be appropriate.

Respectfully submitted,

Date: 2/22/08

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IX. CLAIMS APPENDIX

1. A memory card, comprising:

a substrate having opposed top and bottom surfaces and a plurality of terminals disposed on the bottom surface thereof;

at least one component mounted to the top surface of the substrate and electrically connected to the terminals thereof;

a first encapsulation part formed on the bottom surface of the substrate; and

a second encapsulation part formed on the top surface of the substrate and encapsulating the component mounted thereto, the second encapsulation part being completely separated from the first encapsulation part by the substrate;

the first and second encapsulation parts each being exposed in the memory card.

2. The memory card of Claim 1 wherein the first encapsulation part is formed to include an opening therein, the terminals of the substrate being exposed in the opening.

3. The memory card of Claim 1 wherein:

the second encapsulation part defines an opposed pair of sides; and

a pair of coupling notches are formed in respective ones of the sides of the second encapsulation part in opposed relation to each other.

4. The memory of Claim 1 wherein:

the terminals of the substrate extend in spaced, generally parallel relation to each other;

the second encapsulation part defines an opposed pair of peripheral edge segments which extend in spaced, generally parallel relation to the terminals; and

a pair of guide slots are formed in respective ones of the peripheral edge segments in opposed relation to each other.

5. The memory card of Claim 1 wherein the second encapsulation part includes a recess formed therein adjacent a peripheral edge segment of the second encapsulation part disposed furthest from the terminals.

6. The memory card of Claim 1 wherein the first encapsulation part and the second encapsulation part are each fabricated from an epoxy mold compound.

7. The memory card of Claim 1 wherein:

the first encapsulation part is of a first thickness; and

the second encapsulation part is of a second thickness which exceeds the first thickness.

8. The memory card of Claim 1 comprising multiple components mounted to the top surface of the substrate and electrically connected to the terminals thereof.

9. The memory card of Claim 8 wherein the components are selected from the group consisting of:

a semiconductor package;

a semiconductor die;

a passive component; and

combinations thereof.

10. The memory card of Claim 9 wherein:

the semiconductor package and the passive component are surface mounted to the top surface of the substrate; and

the semiconductor die is wire bonded to the substrate through the use of a conductive wire.

11. A method for fabricating a memory card, the method comprising the steps of:

a) providing a substrate having opposed top and bottom surfaces and a plurality of terminals disposed on the bottom surface thereof;

b) forming a first encapsulation part on the bottom surface of the substrate;

c) mounting at least one component to the top surface of the substrate in a manner wherein the component is electrically connected to the terminals; and

d) forming a second encapsulation part on the top surface of the substrate in a manner encapsulating the component mounted thereto;

the first and second encapsulation parts formed in steps (b) and (d) each being exposed in the memory card and completely separated from each other by the substrate.

12. The method of Claim 11 wherein step (b) comprises forming the first encapsulation part to include an opening therein, the terminals of the substrate being exposed in the opening.

13. The method of Claim 11 wherein step (d) comprises forming a pair of coupling notches into respective ones of an opposed pair of sides of the second encapsulation part in opposed relation to each other.

14. The method of Claim 11 wherein:

step (d) comprises forming a pair of guide slots into respective ones of an opposed pair of peripheral edge segments of the encapsulation part which extend in spaced, generally parallel relation to the terminals.

15. The method of Claim 11 wherein step (d) comprises forming a recess in the second encapsulation part along a peripheral edge segment thereof which is disposed furthest from the terminals.

16. The method of Claim 11 wherein steps (b) and (d) comprise forming the first and second encapsulation parts from an epoxy mold compound.

17. The method of Claim 11 wherein:

step (b) comprises forming the first encapsulation part to be of a first thickness; and

step (d) comprises forming the second encapsulation part to be of a second thickness which exceeds the first thickness.

18. The method of Claim 11 wherein step (c) comprises mounting and electrically connecting a plurality of components to the substrate.

19. The method of Claim 18 wherein step (c) comprises:

1) surface mounting at least one of the components to the substrate; and

2) wire bonding at least one of the components to the substrate.

20. A method for fabricating a memory card, the method comprising the steps of :

a) providing a substrate having opposed top and bottom surfaces and a plurality of terminals disposed on the bottom surface thereof;

b) applying a mold compound to the bottom surface of the substrate;

c) mounting at least one component to the top surface of the substrate in a manner wherein the component is electrically connected to the terminals; and

d) applying a mold compound to the top surface of the substrate in a manner encapsulating the component mounted thereto;

the mold compound applied to the substrate in steps (b) and (d) being exposed in the memory card, with the mold compound applied to the bottom surface being completely separated from the mold compound applied to the top surface by the substrate.

21. A memory card, comprising:

a substrate having opposed top and bottom surfaces and a plurality of terminals disposed on the bottom surface thereof;

at least one component mounted to the top surface of the substrate and electrically connected to the terminals thereof;

a first encapsulation part of a first thickness formed on the bottom surface of the substrate; and

a second encapsulation part of a second thickness exceeding the first thickness formed on the top surface of the substrate and encapsulating the component mounted thereto, the second encapsulation part being completely separated from the first encapsulation part by the substrate;

the first and second encapsulation parts each being exposed in the memory card.

22. A method for fabricating a memory card, the method comprising the steps of :

a) providing a substrate having opposed top and bottom surfaces and a plurality of terminals disposed on the bottom surface thereof;

b) applying a mold compound to the bottom surface of the substrate at a first thickness;

c) mounting at least one component to the top surface of the substrate in a manner wherein the component is electrically connected to the terminals; and

d) applying a mold compound to the top surface of the substrate at a second thickness which exceeds the first thickness and in a manner encapsulating the component mounted thereto;

the mold compound applied to the substrate in steps (b) and (d) being exposed in the memory card, with the mold compound applied to the bottom surface being completely separated from the mold compound applied to the top surface by the substrate.

23. The memory card of Claim 1 wherein the first and second encapsulation parts are configured to impart a prescribed form factor to the memory card.

24. The memory card of Claim 1 wherein the first encapsulation part is sized and configured to cover the entirety of the top surface of the substrate.

X. EVIDENCE APPENDIX

None

XI. APPENDIX OF RELATED PROCEEDINGS

None